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FAULT TOLERANCE IN REVERSIBLE LOGIC CIRCUITS AND QUANTUM COST OPTIMIZATION

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Abstract. Energy dissipation is a prominent factor for the very large scale integrated circuit (VLSI). The reversible logic-based circuit was capable to compute the logic without energy dissipation. Accordingly, reversible circuits are an emerging domain of research based on the low value of energy dissipation. At nano-level design, the critical factor in the logic computing paradigm is the fault. The proposed methodology of fault coverage is powerful for testability. In this article, we target three factors such as fault tolerance, fault coverage and fault detection in the reversible KMD Gates. Our analysis provides good evidence that the minimum test vector covers the 100 % fault coverage and 50 % fault tolerance in KMD Gate.

Further, we show a comparison between the quantum equivalent and controlled V and V^+ gate in all the types of KMD Gates. The proposed methodology mentions that after controlled V and V^+ gate based ALU, divider and Vedic multiplier have a significant reduction in quantum cost. The comparative results of designs such as Vedic multiplier, division unit and ALU are obtained and they are analyzed showing significant improvement in quantum cost.

Keywords: KMD Gate, controlled V and V^+ gate, ALU, divider and Vedic multiplier

1 INTRODUCTION

Launder proved that any irreversible or conventional computation will dissipate $KTln2$ Joules (k is Boltzmann's constant and T is the temperature) of heat since it loses bit information from input to output transition [1]. Bennett introduced a logically reversible computing machine [2].

In reversible logic, the energy dissipation during computation is null, since it has a bijective mapping between input and output. The reversible logic circuits are constructed using a distinguished well-defined library of gates. Good reversible logic circuits must be well optimized in terms of quantum cost (QC), constant input (CI), garbage output (GO) and logical calculations (LC) [3]. The reversible logic circuits are established in quantum cellular automata and optical computation.

The testing of circuits will guarantee the perfect operation. Generally, two major classification of testing: which are online and offline. Testable circuits have their challenges such as test data minimization, low-level signals, variety of fault models [4].

Initially, reversible logic gates/circuits testing in online/offline over the benchmark circuits have been done in [5]. It has been extended towards defining the performance measure parameters like Missing Gate, Cell fault, Stuck-at Fault. Also, two testable reversible gates R1 and R2 are presented for online testing [6].

Thereafter, many researchers had contributed to the reversible fault tolerant architectures such as adders, ALU and floating-point units. Variety of Adders (CSA, RCA, BCD and CLA) are constructed using ZCG, LCG, MIG, Fredkin and F2G parity preserving gates. It is observed that the parity preserving gates provides improved performance in the various adder structures [7]. In RUG gate fault pattern based Fault tolerance is analyzed and it has 52.2 of average fault tolerance on faults. An ALU has been constructed using this reversible gate [8].

Moreover, the synthesis of reversible circuits is a significant part of optimizing performance measures. The quantum reversible circuits are obtained for the basic gates. The quantum circuits can be derived from mapping them to the NCV library [9]. Also, fault models and various approaches towards test pattern generation are discussed here in [9].

In this paper, the fault coverage, fault tolerance and fault detection test vector for the KMD Gates are discussed. Then arithmetic and logic circuit, floating-point division and Vedic multipliers are constructed using KMD Gates. These reversible circuits are optimized in quantum cost using the behavioral model of integrated qubit optimization [10].

The rest of the paper is organized as follows: Section 2 deals with fundamental fault models in reversible logic with an example. Section 3 describes the methods used to reduce the quantum cost in detail; then in Section 4 fault tolerance in KMD Gates is checked. Thereafter, in Section 5, quantum cost optimization in arithmetic circuits such as ALU, division and Vedic multiplier is elaborated. Finally, the conclusion is presented with future scope.

2 PRELIMINARIES OF FAULT MODELS IN REVERSIBLE LOGIC

Faults are any types of imperfection in a system that affects the functional behavior of a system either permanently or temporarily. The fault is caused either by manual or environmental factors. A fault model describes the type of fault that occurred in the system and it identifies the target of testing. There are many types of fault methods [4]:

- Stuck-at fault,
- Bridging fault,
- Missing gate fault,
- Cell fault,
- Cross-point fault.

2.1 Stuck-At Fault

In the stuck-at fault model, the fault occurred in a circuit when any wire fixed on a value '0' or '1', called as stuck-at 0 or stuck-at 1 fault, respectively. Total number of stuck-at faults can be obtained, as shown in Equation (1) [4]

$$2\left(N+\sum_{i=1}^{m} g_i\right) \tag{1}$$

where g_i represents the size of the N^{th} gate of the circuit, N represents the total number of wires and m represents the number of gates in the circuit.

2.2 Minimum Test Vectors

The minimum test vectors are the test vectors covering maximum faults occurring in the reversible circuit.

2.3 Fault Coverage

It is defined as the ratio of the actual number of detected faults to the total number of faults present in the circuits [11]. Based on fault coverage, the efficiency of the testing techniques can be explained as in [11, 12].

fault coverage = (number of detected fault)/(number of detectable fault).

2.4 Fault Tolerance

Fault tolerance is the property of the system that permits a system to work continuously even in the failure of some of its components. The reversible gates with parity preservation are also known as fault tolerant gates [13].

2.5 Controlled V and Controlled V^+ Gates

The V gate is the square root of NOT gate and the V^+ gate is the Hermitian conjugate of the V gate [3, 10]. The V and V^+ gates have the following properties [5, 6]:

$$\begin{aligned} V \times V &= \text{NOT}, \\ V \times V^+ &= V^+ \times V = I, \\ V^+ \times V^+ &= \text{NOT}. \end{aligned} \tag{2}$$

In order to construct a truth table for V and V^+ gates, the properties of these gates are used, as proposed in Equation (2) [3]. This equation shows that when two V gates or two V^+ gates are in series it is equal to a NOT gate. Likewise, when one V and V+ gates are in series, its logical equivalent is identity.

3 QUANTUM COST OPTIMIZATION IN KMD GATES

The Quantum Cost of the reversible logic gate/circuit can be reduced by removing the redundant gates in the quantum equivalent circuits and/or combining the gates in the controlled V and V^+ Structure. At first, the quantum equivalent gate/circuit is obtained from Toffoli-Fredkin Code using the desired expression of the gate/circuit. Then it is decomposed into controlled V and V^+ gate. It is a composition of 2×2 and 1×1 gate of the reversible gate/circuit. The Quantum cost is the sum of the number of 2×2 and 1×1 gates present in the decomposed structure. It is then applied with integrated qubit optimization to remove the redundant gates in the decomposed V and V^+. The process is repeated until further optimization is not possible. The complete process flow graph is shown in Figure 1.

The quantum cost of some of the configurations of the V and V^+ structure is one as shown in Table 1. So, in the controlled V and V^+ structure, wherever these combinations are present it would be considered as one quantum cost. For example,

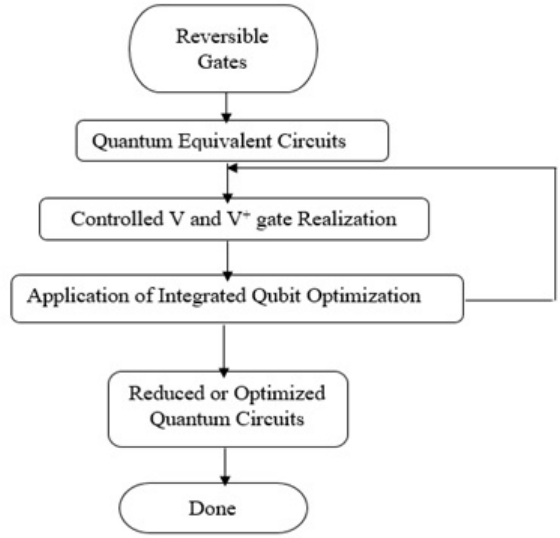

Figure 1. Process flow chart of quantum cost reduction of reversible circuit

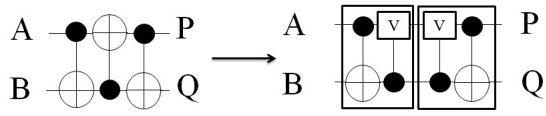

Figure 2. a) C-NOT gates, b) C-NOT gate using controlled V gate

The two controlled-V gates are used instead of single NOT gate. In Figure 2 a) the quantum cost is 3, by rearranging or restructuring using controlled-V gates the quantum cost is reduced to 2. By using this method the quantum cost of any circuit can be reduced. Also, the controlled V and V^+ structures have a reduction in quantum cost in reversible gates and circuits according to the integrated qubit rules [10] are shown in Table 1.

Also, when either two consecutive NOT gate or consecutive controlled V and V^+ gate is present the quantum cost will be zero [3], as shown in Figure 3.

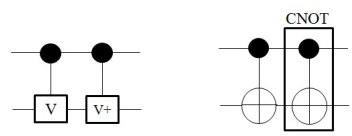

Figure 3. Equivalent circuit having quantum cost as zero

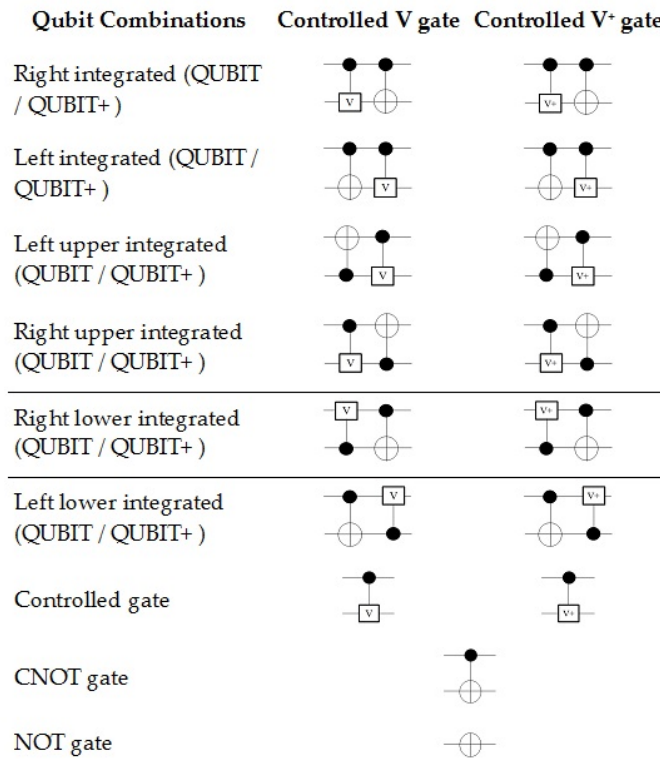

Table 1. Quantum structure of reversible gates with quantum cost = 1 [10]

Using the above two principles the quantum cost of the KMD Gates [14, 15] are optimized as follows.

3.1 KMD Gate1

It is a 3 × 3 gate. In quantum circuit A, B, C represents the input and P, Q, R represents the output. Here in Figure 4 c), there is 9 number of 2 × 2 gates, but according to the constraints [10, 17], the two qubits can be combined. Therefore the quantum cost is 8.

3.2 KMD Gate2

It is a 3 × 3 gate. In quantum circuit A, B, C represents the input and P, Q, R represents the output. Here in Figure 5 c), there is 10 number of 2 × 2 gates, but

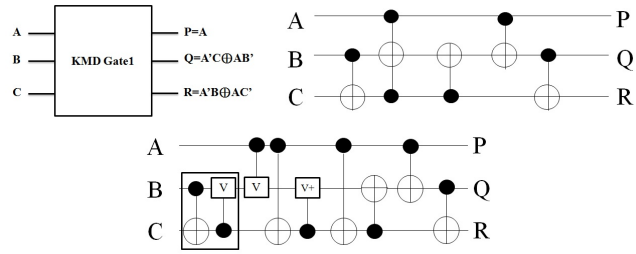

Figure 4. a) Block diagram, b) quantum equivalent, c) V and V^+ gate realization

according to the constraints [10, 17], the two qubits can be combined. Therefore the quantum cost is 9.

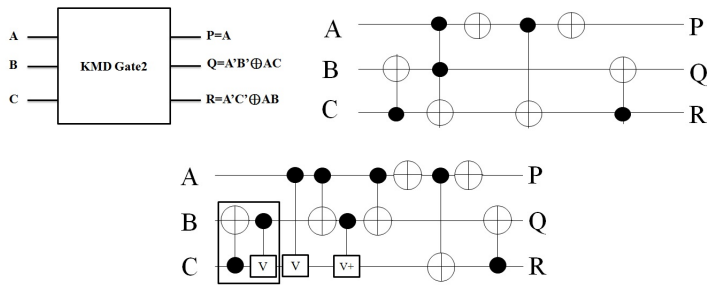

Figure 5. a) Block diagram, b) quantum equivalent, c) V and V^+ gate realization

3.3 KMD Gate3

It is a 4×4 gate. In the quantum circuit, A, B, C, D represents the input and P, Q, R, S represents the output. Here in Figure 6 c), there is 9 number of 2×2 gates, but according to the constraints [10, 17], the two qubits can be combined. Therefore the quantum cost is 8.

3.4 KMD Gate4

It is a 5×5 gate. In the quantum circuit, A, B, C, D, E represents the input and P, Q, R, S, T represents the output. Here in Figure 7 b) there is 24 number of 2×2 gates, but according to rules the two constructive CNOT gate has quantum cost as zero (i.e., canceled). Therefore the quantum cost is 20.

The controlled V and V^+ have a reduction in the quantum cost of reversible gates according to the integrated qubit rules stated in Table 1 using the concepts of [10, 17]. The minimized quantum cost is shown in Table 2. In KMD Gates the quantum cost is reduced in the range of 10 % to 16.67 %.

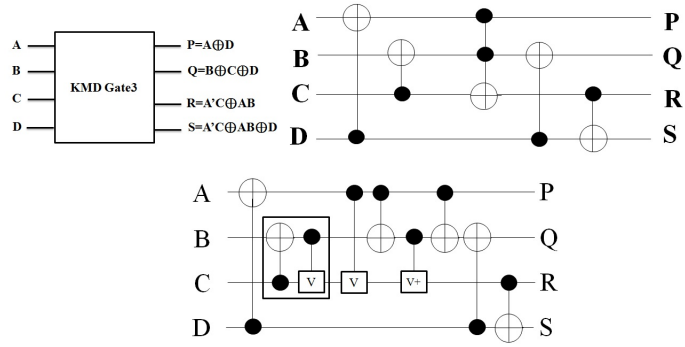

Figure 6. a) Block diagram, b) quantum equivalent, c) V and V^+ gate realization

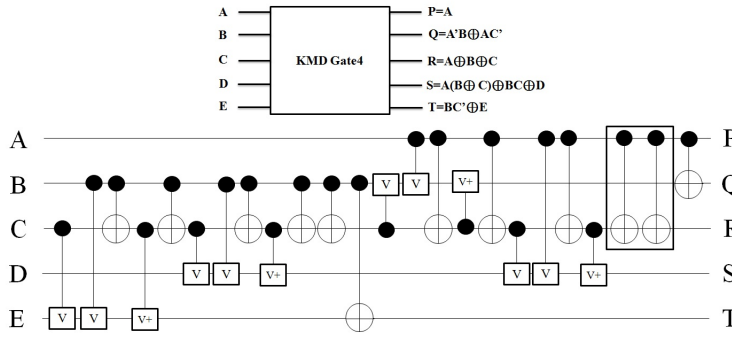

Figure 7. a) Block diagram, b) V and V^+ gate realization

4 FAULT TOLERANCE IN KMD GATES AND CIRCUITS

A reversible gate is said to be parity preserving when the result of XOR operation on input vectors $I_v = I_1, I_2, \ldots, I_n$ is the same as that of the XOR operation on output vectors $O_v = O_1, O_2, \ldots, O_n$, as represented in Equation (3) [7].

Gates	Existing Method [14]	V and V+ gate Realization	% of minimization
KMD Gate1	9	8	11.11%
KMD Gate2	10	9	10%
KMD Gate3	9	8	11.11%
KMD Gate4	24	20	16.67%
MNFT	7	6	14.28%
ZPLG	12	10	16.67%

Table 2. Comparison between quantum equivalent circuit and controlled-V and V^+

$$I_1 \oplus I_2 \oplus \cdots \oplus I_{n-1} \oplus I_n = O_1 \oplus O_2 \oplus \cdots \oplus O_{n-1} \oplus O_n. \quad (3)$$

The test vectors of the circuit or gate are identified using fault table analysis. Using this table, an input capable of covering the maximum number of fault is chosen as the Test vector. A set of test vectors which covers all the fault is known as Test set [13]. This test set is used to check the functionality of the reversible gate whether it is good or faulty. Fault coverage and fault tolerance are estimated for the reversible gate/circuit as shown in Figure 8.

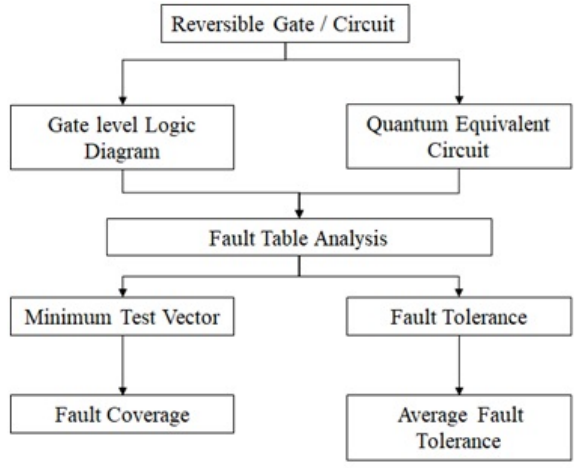

Figure 8. Fault tolerance analysis flow chart

The fault table of the KMD Gate1 is shown in Table 3. The '*' indicates the possible faults that can be detected using the corresponding input test vector. The minimum test vectors to detect all the possible faults are identified from the fault table.

Inputs			Faults																								
A	B	C	a/0	a/1	b/0	b/1	c/0	c/1	d/0	d/1	e/0	e/1	f/0	f/1	g/0	g/1	h/0	h/1	i/0	i/1	j/0	j/1	k/0	k/1	l/0	l/1
0	0	0		*	*		*			*	*			*		*	*		*			*		*		*
0	0	1		*	*		*			*		*		*	*		*		*			*	*			*
0	1	0		*	*			*		*	*		*			*	*		*		*			*	*	
0	1	1		*		*	*		*		*			*	*		*		*		*		*		*	
1	0	0	*			*	*		*			*		*	*		*		*		*		*		*	
1	0	1	*		*		*		*			*		*	*		*		*			*	*			*
1	1	0	*			*		*	*			*	*		*			*	*		*			*	*	
1	1	1	*			*		*	*			*	*		*			*		*	*			*		*
			4	4	4	4	5	3	5	3	3	5	3	5	6	2	6	2	7	1	5	3	4	4	4	4

Table 3. Fault table of KMD Gate1

4.1 Minimum Test Vectors

$$000 - a/1b/0c/0d/1e/0f/1g/1h/0i/0j/1k/1l/1,$$
$$011 - a/1b/1c/0d/0e/0f/1g/0h/0i/0j/0k/0l/0,$$
$$111 - a/0b/1c/1d/0e/1f/0g/0h/1i/1j/0k/1l/1.$$

Here, the three minimum test vectors cover the entire fault in the KMD Gate1. Thus, to detect the fault in the gate;

$$\text{Test Vector} = 000, 011, 111.$$

4.2 Fault Coverage

After removing redundancy from the above minimum test vectors, the possible number of faults can be detected:

$$000 - A/1B/0C/0P/1Q/1R/1 = 6/12,$$
$$011 - Q/0R/0 = 2/12,$$
$$111 - A/0B/1C/1P/0 = 4/12.$$

Stuck-at- faults	Testing position	Test input			Target output			Faulty output		
S-A-0	A	1	1	1	1	0	0	0	1	1
	B	1	1	1	1	0	0	1	1	0
	C	1	1	1	1	0	0	1	0	1
	P	1	1	1	1	0	0	0	0	0
	Q	0	1	1	0	1	1	0	0	1
	R	0	1	1	0	1	1	0	1	0
S-A-1	A	0	0	0	0	0	0	1	1	1
	B	0	0	0	0	0	0	0	0	1
	C	0	0	0	0	0	0	0	1	0
	P	0	0	0	0	0	0	1	0	0
	Q	0	0	0	0	0	0	0	1	0
	R	0	0	0	0	0	0	0	1	1

Table 4. Fault coverage table of KMD Gate1

Hence, all the faults in the KMD Gate1 can be found using the three Test vectors (000, 011 and 111) and their cumulative fault coverage is 100 % as from Table 4. The average fault tolerance of KMD Gate1 is 50 % as shown in Table 5.

ABC	a/0	a/1	b/0	b/1	c/0	c/1	d/0	d/1	e/0	e/1	f/0	f/1	g/0	g/1	h/0	h/1	i/0	i/1	j/0	j/1	k/0	k/1	l/0	l/1	m/0	m/1	n/0	n/1	Fault coverage
000	a0	a7	a0	a1	a0	a2	a0	a3	a0	a2	a0	a7	a0	a3	a0	a2	a0	a3	a0	a1	a0	a4	a0	a3	a0	a2	a0	a1	14/28
001	a2	a6	a2	a3	a0	a2	a2	a1	a0	a2	a2	a5	a2	a1	a0	a2	a1	a2	a3	a2	a2	a6	a1	a2	a0	a2	a2	a3	14/28
010	a1	a5	a0	a1	a1	a3	a2	a1	a3	a1	a1	a6	a2	a1	a3	a1	a1	a2	a0	a1	a1	a5	a1	a2	a1	a3	a0	a1	14/28
011	a3	a4	a2	a3	a1	a6	a0	a3	a3	a1	a3	a4	a0	a3	a3	a1	a0	a3	a3	a2	a3	a7	a0	a3	a1	a3	a2	a3	14/28
100	a0	a7	a7	a5	a7	a6	a7	a4	a7	a6	a0	a7	a7	a4	a7	a5	a7	a4	a7	a6	a3	a7	a4	a7	a5	a7	a6	a7	14/28
101	a2	a6	a6	a4	a7	a6	a6	a5	a7	a6	a1	a6	a5	a6	a4	a6	a6	a5	a7	a6	a2	a6	a5	a6	a4	a6	a6	a7	14/28
110	a1	a5	a7	a5	a5	a4	a6	a5	a4	a5	a2	a5	a5	a6	a7	a5	a6	a5	a4	a5	a1	a5	a5	a7	a5	a7	a4	a5	14/28
111	a3	a4	a6	a4	a5	a4	a7	a4	a4	a5	a3	a4	a7	a4	a4	a6	a7	a4	a4	a5	a0	a4	a4	a6	a4	a6	a4	a5	14/28

Table 5. Fault tolerant table of KMD Gate1

Similarly, it is possible to found out Test vector, fault coverage and fault tolerance for the KMD Gate2, KMD Gate3 and KMD Gate4 as in Table 6. From the table, it is observed that the fault coverage is 100 % for all the KMD Gates and average fault tolerance is approximately 50 %.

The complete processing steps for all the four KMD Gates are made available at online repository (`https://github.com/kamarajvlsi/Reversible_Logic`).

Reversible Gate	Test vectors	Fault Coverage (After redundancy removal)	Average Fault Tolerance
KMD Gate1	000, 011, 111	000 – A/1 B/0 C/0 P/1 Q/1 R/1 = 6/12 011 – Q/0 R/0 = 2/12 111 – A/0 B/1 C/1 P/0 = 4/12	50%
KMD Gate2	000, 100, 011	000 – A/1 B/1 P/1 Q/0 R/0 = 5/12 100 – A/0 B/0 C/0 P/0 Q/1 R/1 = 6/12 011 – C/1 = 1/12	47.32%
KMD Gate3	0000, 0111, 1011	0000 – A/1 B/1 C/0 D/0 P/1 Q/1 R/1 S/1 = 8/16 0111 – A/0 P/0 Q/0 S/0 = 4/16 1011 – B/0 C/1 D/1 R/0 = 4/16	45.42%
KMD Gate4	00000, 00100, 01100, 10111	00000 – A/1 D/1 E/1 P/1 Q/1 R/1 S/1 T/1 = 8/20 00100 – B/1 C/0 D/0 E/0 R/0 = 5/20 01100 – C/1 Q/0 S/0 = 3/20 10111 – A/0 P/0 T/0 = 5/20	40.25%

Table 6. Fault analysis of KMD Gates

5 QUANTUM COST OPTIMIZATION IN ARITHMETIC CIRCUITS

5.1 Arithmetic and Logic Unit

The arithmetic and logic unit constructed in the [14] using the KMD Gates performs 18 distinct operations. The architecture consists of logic gates, adders and multiplexers, as shown in Figure 9. It has a minimum number of control signals and the integrated architecture performs both arithmetic and logical operations in the same structure. In that, two approaches were followed; one is constructing ALU

using KMD Gates alone and another is using KMD, Toffoli and Fredkin Gates. In both approaches, parity preservation is maintained.

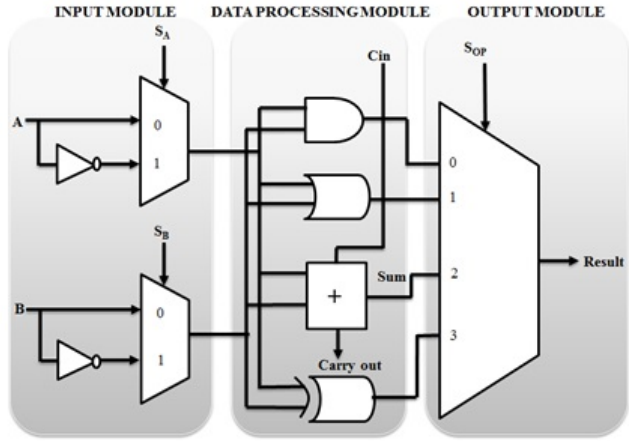

Figure 9. ALU architecture [14]

The overall quantum cost of the integrated ALU is reduced, after applying Integrated qubit optimization as shown in Table 7.

Architecture	ALU (Before V and V+) [14]		ALU (After V and V+ realization)		% of improvement	
Methods	Approach 1	Approach 2	Approach 1	Approach 2	Approach 1	Approach 2
Quantum Cost	116 n	100 n	101 n	92 n	13%	8%
Constant Input	7 n	8n	7n	8n	-	-
Garbage Output	21n	22n	21n	22n	-	-
Number of Gates	64	46	64	46	-	-
Total Cost (QC+CI+GO+NoG)	205	176	193	168	5.85%	4.54%
Logical Calculation	12α + 14β +6??	12α + 14β +6??	12α + 14β +6??	12α + 14β +6??	-	-

Table 7. Quantum cost of ALU before and after controlled-V and V^+ gate realization

5.2 Floating Point Division Unit

The floating-point (FP) operation is a time consuming one in the processor. In [15] a floating-point division unit is proposed with IEEE 754 single-precision format using a non-restoring algorithm. The n-bit FP division consists of the multiplexer, parallel adder and registers. The multi-function register performs, serial-in, parallel in and hold operations as shown in Figure 10.

The percentage of improvement in quantum cost after V and V^+ structure optimization is shown in Tables 8 and 9.

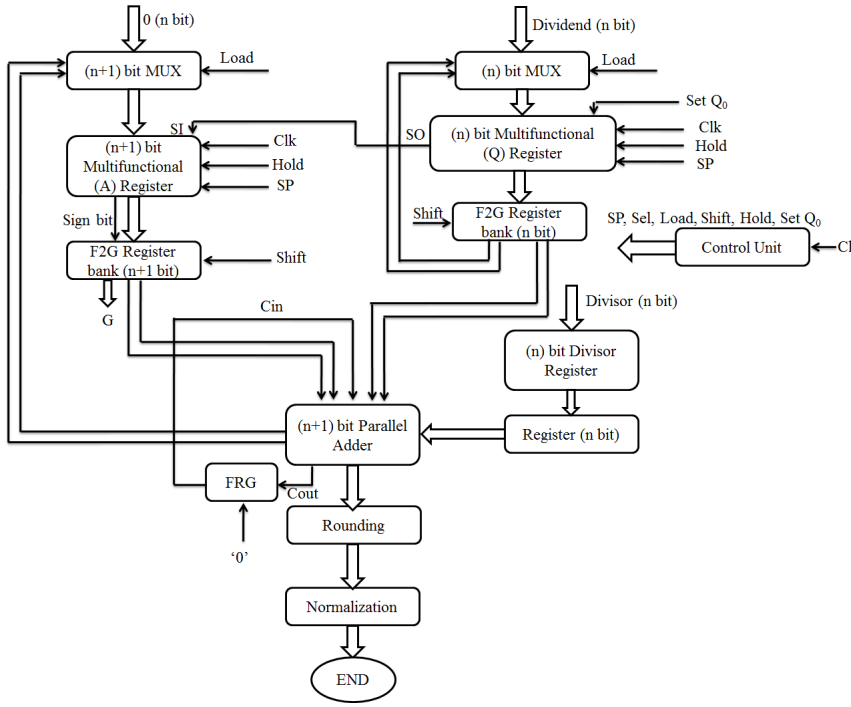

Figure 10. Fault-tolerant floating-point division unit [15]

Modules	No of bits	Gates used	Quantum Cost: Before applying Control V and V+ [15]	Quantum Cost: After applying Control V and V+	% of improvement in Quantum Cost
MUX	n	KMD Gate3	9n	8n	11.12%
	n+1		9n+9	8n+8	11.12%
Multifunctional register	3n		28n	25n	10.72%
	3n+1		28n+28	25n+25	10.72%
Divisor Register	n	F2G	2n	2n	-
Parallel Adder	n+1	KMD Gate4	22n+22	20n+20	9.1%
Register	n	F2G	2n	2n	-
	n+1		2n+2	2n+2	-
Rounding	n+1	KMD Gate3 + F2G	9n+9+2n+2	8n+8+2n+2	11.12%
Normalization	n+1	KMD Gate3	9n+9	8n+8	11.12%
Total Cost of Division			122n+81	110n+73	9.86%

Table 8. Quantum cost of the division unit before and after controlled-V and V^+ gate realization (for n-bit)

No. of bits	Before applying Control V and V+ [15]	After applying Control V and V+	% of reduction in Quantum Cost
1	203	183	9.85%
2	325	293	9.84%
4	569	513	9.84%
8	1,057	953	9.84%
16	2,033	1,833	9.84%
32	3,985	3,593	9.84%
64	7,889	7,113	9.83%
128	15,697	14,153	9.83%
256	31,313	28,233	9.83%

Table 9. Quantum cost of the division unit (1–256 bits)

5.3 Vedic Multiplier (VM)

The 2×2 Vedic multiplier can be constructed using 4 AND gates and 2 half adder, as shown in Figure 11. A 2-bit multiplication of two numbers A.B could be carried out in the following manner, as shown in Equation (4). The logical expression of the 2×2 Vedic multiplier final product is

$$\begin{aligned} P0 &= A0.B0, \\ P1 &= (A1.B0) \oplus (A0.B1), \\ P2 &= (A0.A1.B0.B1) \oplus (A1.B1), \\ P3 &= A0.A1.B0.B1. \end{aligned} \tag{4}$$

The AND gates are constructed using the KMD Gate2 and half adder structure is constructed using KMD Gate3. By fixing $C = 0$ and $D = B$ in the KMD Gate3 the half adder circuit is obtained and the results are taken from P and R in the output side [16].

The quantum cost of the 4×4 Vedic multiplier as shown in Figure 11 is 84 and the constant input is 48. Here the output other than P0, P1, ..., P7 is considered as the garbage output [16]. In order to reduce the quantum cost of the circuit, the controlled V and V+ gate realization is performed as shown in Table 10. After applying integrated qubit principles, the quantum cost of the 4-bit VM is reduced by 10 % and it has an impact on the total cost reduction as 7.4 %.

The complete process and methodology, functional descriptions, simulations in QCA environment and analysis procedure are made available in online repository (`https://github.com/kamarajvlsi/Reversible_Logic`).

6 CONCLUSION

Reversible logic based computing systems consume ideally zero power dissipation. At nano-metric circuit design, the fault detection and fault-tolerant are significant

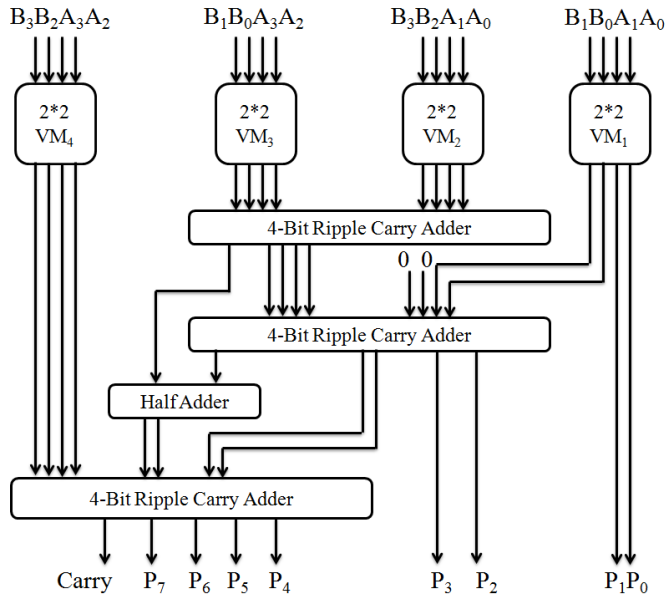

Figure 11. The hardware structure of 4-bit Vedic multiplier [16]

parameters. In the proposed methodology, it has been focused on fault tolerance, fault coverage and fault detection in the reversible KMD Gates. Our analysis provides evidence that minimum test vectors cover the 100 % fault coverage and 50 % fault tolerance in KMD Gates. Further, comparisons between the quantum equivalent and controlled V-V^+ gate for all the types of KMD Gates are shown. The

Module	Garbage Output	Constant Input	No. of Primitive Gates	No. of Gates	Quantum Cost (applying Control V and V⁺ structure)		% of Improvement in Quantum Cost
					Before [16]	After	
AND Gate	2	1	6	1	9	8	11.12%
Half Adder	2	1	5	1	9	8	11.12%
Full Adder	3	2	8	1	22	20	9.1%
2-bit Vedic Multiplier	12	6	34	6	54	48	11.12%
4-bit Ripple Carry Adder	12	8	32	4	88	80	9.1%
4-bit Vedic Multiplier	84	48	232	36	480	432	10%
Total Cost (QC+GO + CI + NoG)					648	600	7.4%

Table 10. Quantum cost of the Vedic multiplier before and after controlled V and V^+ gate realization

controlled V-V+ has been applied to ALU, division and multiplier. It has been observed that the quantum cost has reduced 8–13 %, 9.8 % and 10 % in ALU, floating point division and Vedic multiplier, respectively. It has a good impact on the total cost reduction of 4.5–5.8 % and 7.4 % in ALU and Vedic multiplier. So, we conclude that the quantum cost of the reversible logic circuit can be reduced by applying controlled V–V^+ on them. Further, this work can be incorporated in a processor design in a nano-metric level.

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